

Communications engineering | technology offer

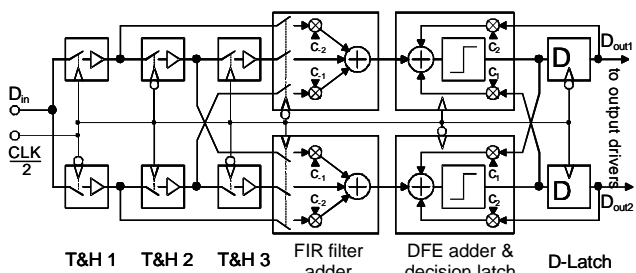
„Bit-rate flexible receive-side equalizer for multi-Gbit/s serial data links“

Field of application

The received signal in high speed serial data links suffers from intersymbol interference. The interference gets more and more severe with increasing data rate over bandwidth limited electrical or optical channels. This problem must be solved, as data rates that exceed 10 Gbit/s per channel by far are expected for the near future. The use of expensive low loss PCB substrates or dispersion corrected glass fibers can be avoided when electronic transmitter predistortion or receiver equalization is used. The improvement of the electronic equalizers with respect to chip area and power consumption (while preserving good equalization characteristics) is a current challenge in the design of new integrated circuits with high throughput serial connectivity. In particular, the transceiver circuitry requirements for serial links with data rates of 10 Gbit/s and more over legacy backplane channels are not easy to fulfill.

Ensure your innovation advantage

A new receive equalizer topology was invented at the University of Stuttgart. The structure invented permits to reduce the equalizer chip area by a factor of 5 to 10 and to cut down power consumption by half compared to common equalizers. At the same time the equalizer exhibits convincing filter properties. A demonstrator of the invention is implemented in a 130 nm standard CMOS technology. The two-fold interleaved equalizer core is reduced to an chip area of $60 \mu\text{m} \times 56 \mu\text{m}$. The power consumption at 10 Gbit/s operation is only 21 mW for the equalizer core and 33 mW for the equalizer clock distribution. The equalizer is able to compensate channel losses up to 24 dB at the Nyquist frequency. The all-clocked topology of the equalizer allows a fully bit-rate flexible operation of the equalizer. The invented architecture allows to scale up the interleaving order of the equalizer core topology for data rates far in excess of 10 Gbit/s if implemented in state-of-the-art CMOS technologies.



Example of an equalizer architecture according to the invention.

The analog demultiplex of the incoming signal at the equalizer input allows a simple interface of the circuit to the following digital functional blocks. The equalizer architecture exhibits a perfect symmetry of all parallel data channels, thus all parallel data streams at the equalizer output have the same quality and are available for further processing without corrections. This receive-side-only equalizer needs no back channel for transmission of equalizer coefficients to a data transmitter predistortion, therefore the design and the operation of the serial link will be greatly simplified.

Your advantages at a glance:

- 5 to 10-times chip area reduction possible compared to traditional equalizer structures
- half the power consumption possible compared to traditional equalizer structures
- 10 Gbit/s operation demonstrated with 130 nm CMOS prototype chip
- Data rates $\gg 10$ Gbit/s can be achieved by higher interleaving order or with faster CMOS technologies
- Bit-rate flexible operation of equalizer
- Complete symmetric equalizer architecture for same signal quality in all parallel data channels
- Receive-side-only equalizer architecture allows for simple design and operation of high-speed serial interfaces

Patent situation

A German patent DE 10 2006 034 033 B3 is granted. A patent application in the USA is pending.

Technology transfer

The Technologie-Lizenz-Büro GmbH (Germany) on behalf of the Universität Stuttgart offers interested companies the opportunity to acquire an appropriate license for this innovative technology. Furthermore, the research group is interested in industry collaboration to undertake further joint developments.

For further information on the „bit-rate flexible equalizer“, please contact Michael Ott at ott@tlb.de

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